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(54) A device having a circuit board for connecting a plurality of IC-chips.

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Des ription

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to an IC-support device having a plurality of multiterminal IC chips, such as a memory card.

2. Description of the Related Art

In recent years, as the capacities of semiconductor memories, e.g. ROM's and RAM's, have b en increased, memory cards in whch a lot of IC chips for these semiconductor memories are packaged upon or within a single substrate, have b en manufactured and used in a wide area of application such as games and process controls.

However, the above IC chips for semiconductor memories have each thirty to fifty connecting terminals, and these connecting terminals are common connecting terminals such as data bus terminals and control bus terminals, with the exception of some individual terminals such as a chip enable terminal. Thus there is a problem of connecting and wiring of these common connecting terminals and individual connecting terminals on a small substrate.

US-A-4320438 discloses a multi-layer ceramic package in which there is provided a base layer, an intermediate layer on which a chip array is provided and an upper layer with there being a further ring layer and a cover layer. The upper surface of the base layer has a conductive pattern thereon and the upper surface of the intermediate layer also has a conducting pattern thereon. The chips are connected together by wire bonding both directly between the chips and to bonding through lands disposed between and separating the chips. Additionally the conductive patterns on the base layer and the intermediate layer are interconnected by through plated metalised holes. Such a conventional wiring structure will hereinafter be described with reference to Figures 1-3 of the accompanying drawings. US-A-4237522 discloses a packaging structure for suppressing electrical noise between chips by providing power sheets perpendicular to the IC packaged substrate. IC chips are arranged in rows on the upper surface of th substrate, each chip being square-shaped and its sides being arranged inclinedly with reference to the row direction.

A conventional wiring structur will now be described with reference to the drawings:

FIG. 1 is a plan view of a conventional memory card; FIG. 2 is a partially plan view illustrating connecting and wiring betw en IC chips of the conventional memory card shown in FIG. 1; and FIG. 3 is a partially sectional view thereof. A substrate 50 which forms a memory card 5 is a double-sided wiring board, as shown in FIG. 3. On an upper surface 50a, twenty IC chips denoted at A_1 to A_{20} are bonded, and upper surface patterns "a" each shown by a solid line, bonding patterns "n" each shown by a black circle and through-hole patterns "m" each shown by a white circle are provided. On the other hand, on a lower surface 50b, lower surface patterns "b" each shown by a dotted line are provided and connected to upper surface 50a by means of through-hole patterns "m".

As shown in FIG. 2, each IC chip "A" is square-shaped, and one pair of corresponding sides "c" and "d" are each provided with connecting terminals while the other pair of corresponding sides "e" and "f" are not provided with any connecting terminal (each side of one IC chip is shown by a dotted line for ease of understanding). All the connecting terminals provided at side "c" are common connecting terminals, and among the connecting terminals provided at side "d", nineteen terminals are common connecting terminals and one terminal is a chip enable terminal.

Connecting and wiring between the above IC chips will be described with reference to A_1, A_2 and A_3.

As shown in FIG. 2, twenty connecting terminals provided at side c_2 of IC chip A_2 are connected to respective bonding patterns n_2, and twenty connecting terminals provided at side d_2 are connected to respective through-hole patterns m_2 each by wire bonding. In a similar way, as for IC chip A_3, connecting terminals at side c_3 are connected to the respective bonding patterns n_3, and connecting terminals at side d_3 are connected to respective through-hole patterns m_3 each by wire bonding. Half (ten in number) of bonding patterns n_2 connected to connecting terminals of IC chip A_2 are connected to respective bonding pattems n_3 connected to the common connecting terminals of IC chip A_3, by means of ten upper surface patterns a_1 which are arranged on the upper part (on the plane of the drawing) of IC chip A_2 so as to avoid the through-hole patterns m_2, and the remaining bonding patterns n_2 are connected to the corresponding bonding patterns m_3 of IC chip A_3 by means of ten upper surface patterns a_2 which are arranged on the lower part (on the plane of the drawing) of IC chip A_2. Furthermore through-h le patterns m_2 connected to connecting terminals of IC chip A_2, are directly connected to through-hole patterns m_3 of IC chip A_3 by means of lower surface pattems "b" arranged on the lower surface of substrate 50.

That is to say, the above-mentioned structure allows connections between common connecting terminals which are provided at one side of each IC chip to be made on upper surface 50a to which IC chips are bonded. On lower surface 50b where no IC chip exists, connections between common connecting terminals provided at the other side of the IC chip are made and at the same time the wiring of an individual connecting terminal is separately made all over the surface.

The above is the connection structure between the respective IC chips. Next, the entire connection structure will be described with reference to FIG. 1.

That is to say, twenty IC chips A_1 to A_{20} are arranged and bonded in four rows on substrate 50 in the arrangement direction, as shown by arrow B. At this time, as shown by arrows, by reversing the direction of IC chips every row, the IC chips can be connected on the same plane without crossing the connections between IC chips throughout each of rows.

As mentioned above, the conventional memory card is designed so that the sides of an IC chip having connecting terminals will be perpendicular to the arrangement direction of IC chips on the substrate. Therefore, wiring between common connecting terminals must be divided into the upper surface and the lower surface of the substrate. As a result, there is a problem that since a costly double-sided print board must be used and a costly process of making through-hole patterns must be conducted, the cost of the entire memory card is raised.

On the other hand, by use of a single-sided print board, it is possible to make all connections between common connecting terminals on the IC chip bonding surface, but this requires considerably wide wiring space at both sides of an IC chip, and therefore, it is necessary to make an arrangement, with the distance between IC chips kept long. As a result, there causes a problem that the number of IC chips being mountable on a single card is limited.

SUMMARY OF THE INVENTION

The object of the present invention is to provide an IC-support device such as a memory card which is free of the above problems, low in cost and has a high packing density.

According to one aspect of this invention, there is provided an IC-memory card comprising:

a lower plate having wiring patterns at least on an upper surface;

an upper plate having upp r surface wiring patterns, said upper plate b ing superimposed on said lower plate; and

a plurality of IC chips mounted on said upper plate, each IC chip having a plurality of connecting terminal groups and a chip enable terminal for selecting the individual IC chips;

wherein said upper plate has at least one opening hole therethrough and some of the connecting terminal groups of said plurality of IC chips being wire-bonded to the wiring patterns on said upper plate, the other of the connecting terminal groups of said plurality of IC chips being connected through the at least one opening hole in said upper plate so as to be wire-bonded directly to the wiring patterns on said lower plate;

wherein said chips are linearly arranged in at least one row, the at least one opening hole in said upper plate is an elongated opening hole having longer sides parallel to the row direction of arrangement of said linearly arranged IC chips, each of said IC chips has the common connecting terminal groups arranged at a first side parallel to the longer sides of said elongated opening hole and at a second side perpendicular to said first side, respectively, said common connecting terminal group at the second side perpendicular to the longer side of said elongated opening hole being wire-bonded to the wiring patterns on said upper plate, and said common connecting terminal group at the first side parallel to the longer side of said elongated opening hole being wire-bonded through said elongated opening hole directly to the wiring patterns on the lower plate.

According to a further aspect of this invention there is provided an IC-memory card comprising:

a lower plate having wiring patterns at least on an upper surface;

an upper plate having upper surface wiring patterns, said upper plate being superimposed on said lower plate; and

a plurality of IC chips mounted on said upper plate and being linearly arranged in at least one row;

wherein an opening hole through said upper plate is provided in a corresponding position to each IC chip on said upper plate; each of said IC chips is substantially square-shaped, has one common connecting terminal group and a chip enable terminal at a first side of the four sides of the square and has another common connecting terminal group at a second side opposite to said first side; the wiring patterns on said upper plate comprises two sets of wiring patterns provided parallel to the row direction; the sides of said IC chips ar arranged inclin dly with reference to the row direction; th first sid of each said IC chip and a third side which is adjacent to the first side and which has no connecting terminal are superimposed on one set of the two sets of wiring patterns on said upper plate; and the second side of said IC chip and a fourth side which is adjacent to the

second side and has no connecting terminal are superimposed on th other set of the two sets of wiring patterns on said upper plate; and wherein said one common connecting terminal group at the first side of said IC chip and the other common connecting terminal group at the second side opposite to the first side are wire-bonded to said two sets of wiring patterns on the upper plate respectively, and each of said IC chip enable terminals is wire-bonded through a respective one of said opening holes directly to each of the wiring patterns on the lower plate.

Advantageously on the upper plate, a seal frame is provided for enclosing the plurality of IC chips, and a resin is injected inside the seal frame.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of a conventional memory card;

Figures 2 and 3 are a partially plan view and a partially sectional view both of the memory card shown in Figure 1;

Figure 4 is a plan view of a first embodiment of a memory card according to the present invention;

Figures 5 and 6 are a partially plan view and a partially sectional view of the memory card shown in Figure 4;

Figure 7 is a plan view of a second embodiment of a memory card according to the present invention;

Figures 8 and 9 are sectional views taken along A-A and B-B respectively of the memory card shown in Figure 7;

Figures 10 and 11 are a top plan view and a bottom plan view both of the lower plate of the second embodiment;

FIG. 12 is a plan view of the upper plate of the second embodiment; and

FIG. 13 and 14 are plan views of seal frames used in the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now b described in detail with reference to the drawings.

FIG. 4 is a plan view of a first embodiment of a memory card according to the present invention; FIG. 5 is a partial plan view illustrating the connecting and wiring between IC chips; and FIG. 6 is a partial sectional vi w th r of.

As shown in FIG. 6, a substrate 1 which forms a memory card, comprises a lamination of an upper plat 2 and a lower plate 3 both made of a singl -sided print board. Pattern surface 2a of upper plate 2 is provided with upper surface patterns "P", bonding patterns "n" and opening holes "h", all of which are shown by solid lines, while pattern surface 3a of the lower plate 3 is provided with lower surface patterns "q" shown by dotted lines and bonding patterns "o" which are respectively placed in positions corresponding to opening holes "h" in upper plate 2.

And as shown in FIG. 4, twenty IC chips A_1 to A_{20} are bonded on pattern surface 2a of the above upper plate 2 in such a manner that the respective sides c, d, e and f of each IC chip are inclined with reference to the direction of arrangement shown by arrow B.

Connecting and wiring between the above IC chips will be described in relation to IC chips A_2 and A_3. As shown in FIG. 5, nineteen common connecting terminals provided at side c_2 of IC chip A_2 are each wire-bonded to each of bonding patterns n_2, and one chip enable terminal is bonded via one opening hole h in upper plate 2 to bonding pattern o_2 of lower plate 3. Also, twenty common connecting terminals provided at side d_2 are connected to respective bonding patterns n'_2 each by wire bonding.

In a similar manner, as for IC chip A_3, each connecting terminal at side c_3 is wire-bonded to each bonding pattern n_3 and o_3, and each connecting terminal at side d_3 is wire-bonded to each bonding pattern n'_3. As a result, bonding patterns n_2 connected to connecting terminals of IC chip A_2 are connected to bonding patterns n_3 connected to common connecting terminals of IC chip A_3 adjacent to A_2, by means of nineteen upper surface patterns P_1 which pass the lower surface of IC chip A_2 and are led out of side e_2. This side e_2 has no connecting terminal. Also, bonding patterns n'_2 are connected to bonding patterns n'_1 of adjacent IC chip A_1, by means of twenty upper surface patterns P_2 which pass the lower surface of IC chip A_2 and are led out of side f_2 having no common connecting terminal. That is to say, the above-mentioned structure is designed so that connections between many common connecting terminals are made on pattern surface 2a of upper plate 2 to which IC chips A are bonded, and that connecting and wiring of a small number of individual connecting terminals are separately made all over pattern surface 3a of lower plate 3 where no IC chip exists.

As a result, this inclined arrangement of IC chips allows the wiring patterns between common connecting terminals to be arranged in a substantially linear shape. Also as for connecting and wiring from the upper surface to the lower surface of the substrate, although th prior art has required a large number of connections and wir s, the present invention uses only connections of a small number

of individual connecting terminals. Therefore, it is possible to perform a wire bonding by providing opening holes larger than usual without providing through-hole patterns.

As mentioned above, in the first embodiment of the present invention, a substrate is made of a lamination of low-cost single-sided print boards, and connections between common connecting terminals which are large in number are made on the upper plate, while individual connecting terminals which are small in number are connected via opening holes to the lower plate.

Also, the inclined arrangement of IC chips on the substrate allows connections between common connecting terminals to be made on one surface of the substrate without increasing the space for arrangement of IC chips. Therefore, a memory card having a high packing density can be provided by low-cost single-sided boards. At the same time, eliminating multiterminal through-hole patterns which are apt to cause problems leads to an improvement of reliability.

FIG. 7 is a plan view of a second embodiment of a memory card according to the present invention; FIGS. 8 and 9 are sectional views taken along VIII-VIII and IX-IX, respectively of the memory card shown in FIG. 7; FIGS. 10 and 11 are a top plan view and a bottom plan view both of the lower plate of this embodiment; FIG. 12 is a plan view of the upper plate of this embodiment; and FIG. 13 is a plan view of a seal frame.

As shown in FIGS. 8 and 9, a substrate 1 which forms a memory card 10, comprises a structure in which an upper plate 2 made of a single-sided print board is laminated on an upper surface of a lower plate 3 made of a conventional double-sided print board. A pattern surface 2a of upper plate 2 is, as shown in FIGS. 7 and 12, provided with lead patterns P_1, bonding patterns n, two elongated opening holes H_1 and H_2 and an elongated opening hole H_3 for connecting leads are provided. Along each of longer sides of two elongated opening holes H_1 and H_2, twenty IC chips B_1 to B_{20} are arranged. Among the four sides of IC chip square, at one side along each of the longer sides of the elongated opening holes H_1 and H_2 and at a second side which is perpendicular to the above one side, connecting terminals for each IC chip are provided by halves respectively. Also, as shown in FIG. 10, on upper pattern surface 3a of the lower plate 3, lead patterns P_2 and bonding patterns n and connecting electrodes q_1 are provided, and, as shown in FIG. 11, on low r pattern surface 3b of the low r plate 3, lead patterns P_3, individual lead patterns P_4 and connecting electrodes q_2 are provided, and upper pattern surfac 3a and lower pattern surface 3b are connected by through-hole patterns m.

Next, connecting and wiring between IC chips will be d scribed about IC chips B_{10}, B_{19} and B_{20}. That is to say, as illustrated by IC chip B_{20} in FIG. 7, common connecting terminals provided at side C_{20} perpendicular to the longer sides of the elongated opening hole H_1 is wire-bonded to bonding patterns n_{20} provided on pattern surface 2a of upper plate 2 and thus connected to bonding patterns n_{19} of adjacent IC chip B_{19} and to bonding patterns n_0 for connection between plates by means of lead patterns P_1.

By wire-bonding each IC chip to patterns P_1 shown in FIG. 12, the common connecting terminals of all IC chips are connected in common.

Furthermore by wire-bonding the bonding patterns n_0 for connection between plates, via elongated opening hole H_3, to the upper pattern surface of the through-hole patterns m_0 provided in lower plate 3, as shown in FIG. 11, the above-mentioned common connecting terminals of all IC chips are connected to connecting electrodes q_2 by means of lead patterns P_3 provided on lower pattern surface 3b.

Also, in IC chip B_{20}, the common connecting terminals among connecting terminals provided at its side e_{20} which is parallel to the longer sides of the elongated opening hole H_1 are wire-bonded, via elongated opening hole H_1, to bonding patterns n_{20} provided on upper pattern surface 3a of lower plate 3 and thus connected to bonding patterns n_{10} and n_{11} for adjacent IC chips B_{10} and B_{11} by means of lead patterns P_2 (FIG. 10).

And by wire-bonding each IC chip to lead patterns P_2 as shown in FIG. 10, the common connecting terminals of all IC chips are connected in common and at the same time they are connected to connecting electrodes q_1.

Also one chip enable terminal of each chip included in the above-mentioned side e_{20} (FIG. 7) is wire-bonded to the upper pattern surface of through-hole pattern m_{20} provided in lower plate 3 via elongated opening hole H_1 and thus connected to connecting electrode q_2 by individual lead pattern P_4 provided on lower pattern surface 3b of lower plate 3.

As mentioned above, in connection for a board which is packed with many IC chips, by wire-bonding via elongated opening holes, the number of through-hole patterns can be greatly reduced. As a result, the reliability of an IC-packaged device having high packing density can be enhanced and simultaneously wiring freedom on each plate can be increased.

Wh n comparing the number of through-hole patterns in the package structure of this embodiment with those in the conventional package structure shown in FIG. 1, for twenty IC chips, the conv ntional structure requires tw nty through-

hole patterns per IC chip and thus requires 20 x 20 = 400 through-hole patt rns in total, but this embodiment of the present invention requires through-hole patterns for the common connecting terminals, i.e. twenty through-hole patterns m_0 and a through-hole pattern m_1 to m_{20} for a chip enable terminal necessary for each IC chip and thus requires 20 + 20 = 40 in total, thereby reducing the number of through-hole patterns to 1/10.

Thus, packing and connecting of IC chips have been completed. Next, protection will be described for IC chips and wires. As shown in FIGS. 7 and 8, a seal frame 20 (FIG. 13) is set on pattern surface 2a of upper plate 2 and a seal resin 30 (FIGS. 8 and 9) is injected into the inside of seal frame 20, thereby sealing the package portions of IC chips and the wire-bonded portions by resin.

FIG. 14 shows another embodiment of the seal frame. By providing a partition frame 40a in the center of the seal frame 40, the seal frame 40 is divided into a plurality of small-area seal frame portions. As a result, the recession in the middle portion of the injected seal resin is reduced, thereby making it possible to improve the effect of protection by seal.

In this regard, the partition frame 40a is not limited to the single number. If space of arrangement of IC chips is allowed, partition frames can be provided vertically and horizontally to enhance the effect of protection.

As mentioned above, by use of the seal frame enclosing the entire memory card board, the IC chips, bonding wires and wiring patterns are simultaneously sealed by resin. Thus a highly reliable memory card can be provided.

Thus the foregoing are the embodiments of the present invention. In either embodiment, the upper plate has only the upper surface wiring patterns (single-sided wiring) and opening holes and does not use a so-called through hole pattern. Also, the lower plate minimizes the number of through hole patterns. Therefore, the present invention provides low-cost but highly reliable and highly densed IC memory cards.

Claims

1. An IC-memory card comprising:

   a lower plate (3) having wiring patterns (P2) at least on an upper surface;

   an upper plate (2) having upper surface wiring patterns (P1), said upper plate (2) being superimposed on said lower plate (3); and

   a plurality of IC chips (B1-B20) mounted on said upper plate (2), each IC chip having a plurality of connecting terminal groups and a chip enable terminal for selecting the individual IC chips;

   wherein said upper plat (2) has at least one opening hole (H) therethrough and some of the connecting terminal groups of said plurality of IC chips being wire-bonded to the wiring patterns (P1) on said upper plate, the other of the connecting terminal groups of said plurality of IC chips being connected through the at least one opening hole (H) in said upper plate so as to be wire-bonded directly to the wiring patterns (P2) on said lower plate;

   wherein said chips are linearly arranged in at least one row, the at least one opening hole (H) in said upper plate (2) is an elongated opening hole having longer sides parallel to the row direction of arrangement of said linearly arranged IC chips, each of said IC chips (B1-B20) has the common connecting terminal groups arranged at a first side (e) parallel to the longer sides of said elongated opening hole and at a second side (c) perpendicular to said first side, respectively, said common connecting terminal group at the second side (c) perpendicular to the longer side of said elongated opening hole being wire-bonded to the wiring patterns (P1) on said upper plate, and said common connecting terminal group at the first side (e) parallel to the longer side of said elongated opening hole being wire-bonded through said elongated opening hole (H) directly to the wiring patterns (P2) on the lower plate.

2. The IC-support device according to claim 1 wherein said IC chip has the chip enable terminal arranged at said first side (e) parallel to the longer side of said elongated opening hole (H), said chip enable terminal being wire-bonded directly to the wiring pattern (P2) on the lower plate through said elongated opening hole (H).

3. The IC-support device according to claim 1 having said plurality of IC chips (B1-B20) arranged in a plurality of rows; comprising accordingly a plurality of generally rectangular opening holes (H1, H2); and the wiring patterns on the upper plate (2) where said IC chip rows are mounted, being arranged generally parallel to the longer sides of the elongated opening holes (H1, H2) so that the wiring patterns extend continuously along the longer sides of said plurality of elongated opening holes.

4. The IC-support device according to claim 3 wherein the wiring patterns (P2) on said lower plate (3) are arranged generally in a direction perpendicular to the wiring patterns (P1) on

said upper plate (2).

5. The IC-support device according to claim 1 wherein said upper plate (2) further comprises another opening hole (H3) for directly wire-bonding bonding patterns (nO) of the wiring patterns (P1) on the upper plate (2) to connecting terminals (mO) of the wiring patterns on the lower plate (3).

6. An IC-memory card comprising:
a lower plate (3) having wiring patterns (q) at least on an upper surface;
an upper plate (2) having upper surface wiring patterns (P), said upper plate (2) being superimposed on said lower plate (3); and
a plurality of IC chips (A1-A20) mounted on said upper plate (2) and being linearly arranged in at least one row;
wherein an opening hole (h) through said upper plate (2) is provided in a corresponding position to each IC chip on said upper plate (2); each of said IC chips (A1-A20) is substantially square-shaped, has one common connecting terminal group and a chip enable terminal at a first side (c) of the four sides of the square and has another common connecting terminal group at a second side (d) opposite to said first side; the wiring patterns on said upper plate comprises two sets of wiring patterns (P1, P2) provided parallel to the row direction; the sides of said IC chips (A1-A20) are arranged inclinedly with reference to the row direction; the first side (c) of each said IC chip and a third side (e) which is adjacent to the first side and which has no connecting terminal are superimposed on one set (P1) of the two sets of wiring patterns on said upper plate; and the second side (d) of said IC chip and a fourth side (f) which is adjacent to the second side and has no connecting terminal are superimposed on the other set (P2) of the two sets of wiring patterns on said upper plate; and wherein said one common connecting terminal group at the first side of said IC chip and the other common connecting terminal group at the second side opposite to the first side are wire-bonded to said two sets of wiring patterns (P1, P2) on the upper plate respectively, and each of said IC chip enable terminals is wire-bonded through a respective one of said opening holes (h) directly to each of the wiring patterns (q) on the lower plate (3).

7. The IC-support device according to claim 1 or 6 wherein on the upper plate a seal frame (20) is provided for nclosing said plurality of IC chips, and a r sin (30) is injected insid said seal frame.

Patentansprüche

1. IC-Speicherkarte, die folgendes umfaßt:
eine untere Platte (3) mit mindestens auf einer Oberseite befindlichen Verdrahtungsstrukturen (P2);
eine obere Plätte (2) mit Verdrahtungsstrukten (P1) auf der Oberseite, wobei die obere Platte (2) die untere Platte (3) überlagert; und
eine Vielzahl von auf der oberen Platte (2) eingesetzten IC-Chips (B1-B20), wobei jedes IC-Chip über eine Vielzahl von Anschlußklemmengruppen sowie über einen Chip-Freigabeanschluß zur Anwahl der einzelnen IC-Chips verfügt;
dadurch gekennzeichnet, daß die obere Platte (2) mit mindestens einer Durchgangsöffnung (H) ausgeführt ist, und einige der Anschlußklemmengruppen der Vielzahl von IC-Chips mit den Verdrahtungsstrukturen (P1) der oberen Platte drahtkontaktiert sind, während die anderen Anschlußklemmengruppen der Vielzahl von IC-Chips durch mindestens eine Durchgangsöffnung (H) in der oberen Platte geführt sind, um unmittelbar mit den Verdrahtungsstrukturen (P2) der unteren Platte drahtkontaktiert zu werden;
daß die Chips linear in mindestens einer Reihe angeordnet sind, die mindestens eine Durchgangsöffnung (H) in der oberen Platte (2) in Form eines Langlochs ausgebildet ist, dessen längere Seiten parallel zur Erstreckungsrichtung der Reihe der linear angeordneten IC-Chips verlaufen, und jedes der IC-Chips (B1-B20) über eine an einer ersten Seite (e) parallel zu den längeren Seiten der Langloch-Durchgangsöffnung bzw. an einer zweiten senkrecht zur ersten Seite liegenden Seite (c) angeordnete gemeinsame Anschlußklemmengruppe verfügt, wobei die gemeinsame Anschlußklemmengruppe an der zweiten senkrecht zur längeren Seite der Langloch-Durchgangsöffnung verlaufenden Seite (c) mit den Verdrahtungsstrukturen (P1) auf der oberen Platte drahtkontaktiert ist, und wobei die gemeinsame Anschlußklemmengruppe an der ersten parallel zur längeren Seite der Langloch-Durchgangsöffnung verlaufenden ersten Seit (e) durch di Langloch-Durchgangsöffnung (H) direkt mit den V rdrahtungsstrukturen (P2) auf der unteren Platte drahtkontaktiert ist.

2. IC-Trägervorrichtung gemäß Anspruch 1, dadurch gekennzeichnet, daß d r Chip-Frei-

gabeanschluß des IC-Chip an der ersten parallel zur längeren Seite der Langloch-Durchgangsöffnung (H) verlaufenden Seite (e) angeordnet ist, wobei der Chip-Freigabeanschluß mit der Verdrahtungsstruktur (P2) auf der unteren Platte (2) durch die Langloch-Durchgangsöffnung (H) direkt drahtkontaktiert ist.

3. IC-Trägervorrichtung gemäß Anspruch 1 mit der in einer Vielzahl von Reihen angeordneten Vielzahl von IC-Chips (B1-B20); umfassend eine entsprechende Vielzahl von im allgemeinen rechteckigen Durchgangsöffnungen (H1, H2); sowie mit den Verdrahtungsstrukturen auf der oberen Platte (2), auf der die IC-Chip-Reihen so angeordnet sind, daß sie im allgemeinen parallel zu den längeren Seiten der Langloch-Durchgangsöffnungen (H1, H2) verlaufen, so daß sich die Verdrahtungsstrukturen kontinuierlich entlang der längeren Seiten der Vielzahl von Langloch-Durchgangsöffnungen erstrecken.

4. IC-Trägervorrichtung gemäß Anspruch 1, dadurch gekennzeichnet, daß die Verdrahtungsstrukturen (P2) auf der unteren Platte (3) im allgemeinen in einer Richtung senkrecht zu den Verdrahtungsstrukturen (P1) auf der oberen Platte (2) angeordnet sind.

5. IC-Trägervorrichtung gemäß Anspruch 1, dadurch gekennzeichnet, daß die obere Platte (2) ferner eine weitere Durchgangsöffnung (H3) zur direkten Drahtkontaktierung von Kontaktierungsstrukturen (40) der Verdrahtungsstrukturen (P1) auf der oberen Platte (2) mit den Anschlußklemmen (mO) der Verdrahtungsstrukturen auf der unteren Platte (3) enthält.

6. IC-Speicherkarte, die folgendes umfaßt:
eine untere Platte (3) mit mindestens auf einer Oberseite befindlichen Verdrahtungsstrukturen (q);
eine obere Platte (2) mit Verdrahtungsstrukten (P) auf der Oberseite, wobei die obere Platte (2) die untere Platte (3) überlagert; und
eine Vielzahl von auf der oberen Platte (2) eingesetzten und in mindestens einer Reihe linear angeordneten IC-Chips (A1-A20);
dadurch gekennzeichn t, daß ein Durchgangsöffnung (h) durch di obere Platte (2) an iner jedem IC-Chip auf der oberen Platte (2) entsprechenden Position vorgesehen ist; jedes der IC-Chips (A1-A20) im wes ntlichen quadratisch geformt ist, eine gemeinsame Anschlußklemmengruppe sowi inen Chip-Freigabeanschluß an einer ersten Seite (c) der vier S iten des Quadrats sowi ein w iter gemeinsame Anschlußklemmengruppe an einer zweiten, der ersten Seite gegenüberliegenden Seite (d) besitzt; die Verdrahtungsstrukturen auf der oberen Platte zwei Sätze von parallel zur Erstreckungsrichtung der Reihe verlaufenden Verdrahtungsstrukturen (P1, P2) umfassen; die Seiten der IC-Chips (A1-A20) bezogen auf die Erstreckungsrichtung der Reihe geneigt angeordnet sind; die erste Seite (c) jedes IC-Chips und eine dritte an die erste Seite angrenzende und ohne Anschlußklemme ausgeführte Seite (e) einen Satz (P1) der beiden Satz Verdrahtungsstrukturen auf der oberen Platte überlagern; und die zweite Seite (d) des IC-Chips und eine vierte an die zweite Seite angrenzende und ohne Anschlußklemme ausgeführte Seite (f) den anderen Satz (P2) der beiden Satz Verdrahtungsstrukturen auf der oberen Platte überlagern; und daR die eine gemeinsame Anschlußklemmengruppe an der ersten Seite des IC-Chips und die andere gemeinsame Anschlußklemmengruppe an der zweiten, der ersten Seite gegenüberliegenden Seite mit den beiden Sätzen von Verdrahtungsstrukturen (P1, P2) auf der oberen Platte drahtkontaktiert sind, und jeder der IC-Chip-Freigabeanschlüsse durch eine entsprechende der Durchgangsöffnungen (h) direkt mit jeder der Verdrahtungsstrukturen (q) auf der unteren Platte (3) drahtkontaktiert ist.

7. IC-Trägervorrichtung gemäß Anspruch 1 oder 6, dadurch gekennzeichnet, daß auf der oberen Platte ein dichtes Gehäuse (20) zur Kapselung der Vielzahl von IC-Chips vorgesehen ist und ein Harz (30) in das Innere des dichten Gehäuses eingespritzt wird.

Revendications

1. Carte de mémoire à circuit intégré comprenant :

une plaque inférieure (3) comportant des configurations de câblage (P_2) au moins sur une surface supérieure ;

une plaque supérieure (2) comportant des configurations de câblage de surface supérieure (P_1), la dite plaque supérieure (2) étant superposée à ladite plaque inférieure (3) ; et

un pluralité de puces de circuit intégré CI (B_1-B_{20}) monté s sur ladit plaque supérieure (2), chaque puce de CI comportant une pluralité de groupes de bornes de connexion et une borne d'activation de puce pour la sélection des puces de CI individuelles ;

dans laquelle ladite plaque supéri ure

(2) comporte au moins une ouverture trav r-sante (H) et certains des groupes de bornes de connexion de ladite pluralité de puces de CI sont reliés par fils aux configurations de câblage (P_1) de ladite plaque supérieure, les autres des groupes de bornes de connexion de ladite pluralité de puces de CI étant connectées, à travers ladite au moins une ouverture traversante (H) de ladite plaque supérieure, de façon à être reliés par fils directement aux configurations de câblage (P_2) sur ladite plaque inférieure ; et

dans laquelle lesdites puces sont agencées linéairement en au moins une rangée, ladite au moins une ouverture traversante (H) de ladite plaque supérieure (2) est une ouverture allongée ayant des grands côtés parallèles à la direction de rangée de l'agencement desdites puces de CI agencées linéairement, chacune desdites puces de CI (B_1-B_{20}) comporte les groupes de bornes de connexion commune sur un premier côté (e) parallèle aux grands côtés de la dite ouverture allongée et sur un deuxième côté (c) perpendiculaire audit premier côté, respectivement, ledit groupe de bornes de connexion commune situé sur le deuxième côté (c) perpendiculaire au grand côté de ladite ouverture allongée étant relié par fil aux configurations de câblage (P_1) prévues sur ladite plaque supérieure, et ledit groupe de bornes de connexion commune situé sur le premier côté (e) parallèle au grand côté de ladite ouverture allongée étant relié par fil à travers ladite ouverture allongée (H) directement aux configurations de câblage (P_2) prévues sur la plaque inférieure.

2. Dispositif support de circuit intégré suivant la revendication 1, dans lequel la borne d'activation de puce de ladite puce de CI est placée sur ledit premier côté (e) parallèle au grand côté de la dite ouverture allongée (H), ladite borne d'activation de puce étant reliée par fil directement à la configuration de câblage (P_2) prévue sur la plaque inférieure, à travers ladite ouverture allongée (H).

3. Dispositif support de circuit intégré suivant la revendication 1, portant ladite pluralité de puces de CI (B_1-B_{20}) agencées en une pluralité de rangées, dans lequel il est prévu de façon correspondante une pluralité d'ouvertures sensiblement rectangulaire (H_1,H_2), t les configurations de câblage sur la plaque supérieure (2), sur laquelle sont montées les dites rangées de puces d CI, sont agencées sensiblement parallèlement aux grands côtés des ouvertures traversantes allongées (H_1,H_2) de sort qu les configurations de câblage s'étendent de façon continu l long d s grands côtés de ladite pluralité d'ouv rtures allongées.

4. Dispositif support de circuit intégré suivant la revendication 3, dans lequel les configurations de câblage (P_2) sur ladite plaque inférieure (3) sont agencées sensiblement dans une direction perpendiculaire aux configurations de câblage (P_1) sur ladite plaque supérieure (2).

5. Dispositif support de circuit intégré suivant la revendication 1, dans lequel ladite plaque supérieure (2) comprend en outre une autre ouverture traversante (H_3) pour la liaison directe par fil des configurations de liaison (n_0) des configurations de câblage (P_1) prévues sur la plaque supérieure (2) aux bornes de connexion (m_0) des configurations de câblage prévues sur la plaque inférieure (3).

6. Carte de mémoire à circuit intégré comprenant :

une plaque inférieure (3) comportant des configurations de câblage (q) au moins sur une surface supérieure ;

une plaque supérieure (2) comportant des configurations de câblage de surface supérieure (P), ladite plaque supérieure (2) étant superposée à ladite plaque inférieure (3) ; et

une pluralité de puces de CI (A_1-A_{20}) montées sur ladite plaque supérieure (2) et agencées linéairement en au moins une rangée ;

dans laquelle une ouverture traversante (h) à travers ladite plaque supérieure (2) est prévue dans une position correspondant à chaque puce de CI sur la dite plaque supérieure (2) ; chacune desdites puces de CI (A_1-A_{20}) est de forme sensiblement carrée, comporte un premier groupe de bornes de connexion commune et une borne d'activation de puce sur un premier côté (c) des quatre côtés du carré, et comporte un autre groupe de bornes de connexion commune sur un deuxième côté (d) opposé audit premier côté ; les configurations de câblage sur ladite plaque supérieure comprennent deux ensembles de configurations de câblage (P_1, P_2) parallèles à la direction des rangées ; les côtés des dits puces de CI (A_1-A_{20}) sont inclinés par rapport à la direction des rangées ; l pr mier côté (c) de chaque dite puce de CI et un troisième côté (e) qui est adjacent au premier côté et qui ne porte pas d borne de connexion sont superposés à un premier ensemble (P_1) des d ux ensembles de configu-

rations de câblage prévus sur ladite plaque supérieure ; et le deuxième côté (d) de ladite puce de CI et un quatrième côté (f) qui est adjacent au deuxième côté et ne porte pas de borne de connexion sont superposés à l'autre ensemble (P_2) des deux ensembles de configurations de câblage prévus sur ladite plaque supérieure ; et

dans laquelle ledit premier groupe de bornes de connexion commune sur le premier côté de ladite puce de CI et l'autre groupe de bornes de connexion commune sur le deuxième côté opposé au premier côté sont reliés par fils aux dits deux ensembles de configurations de câblage (P_1,P_2) prévus sur la plaque supérieure, respectivement , et chacune des dites bornes d'activation de puce de CI est reliée par fil à travers une ouverture respective desdites ouvertures traversantes (h) directement à chacune des configurations de câblage (q) prévues sur la plaque inférieure (3).

7. Dispositif support de circuit intégré suivant la revendication 1 ou 6, dans lequel un cadre de fermeture (20) est prévu sur la plaque supérieure pour entourer la pluralité de puces de CI et une résine (30) est injectée dans le cadre de fermeture.

FIG. 1
(PRIOR ART)

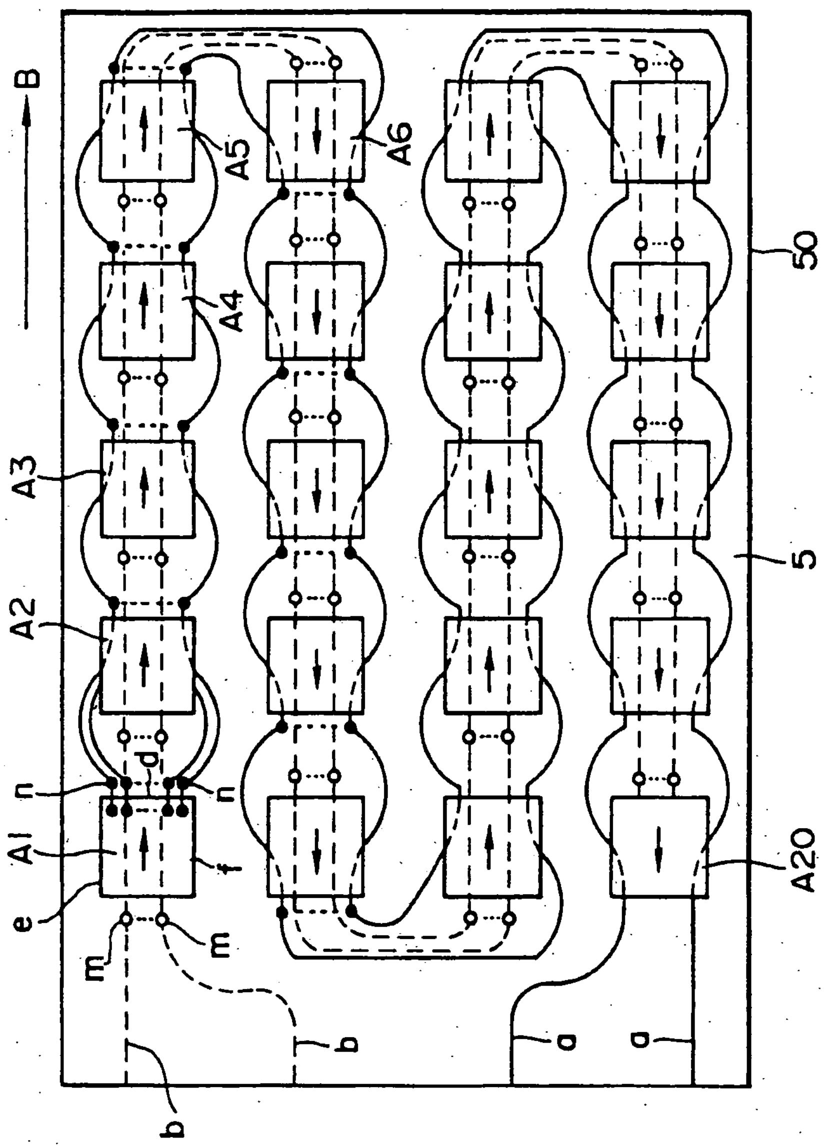


FIG.2
(PRIOR ART)

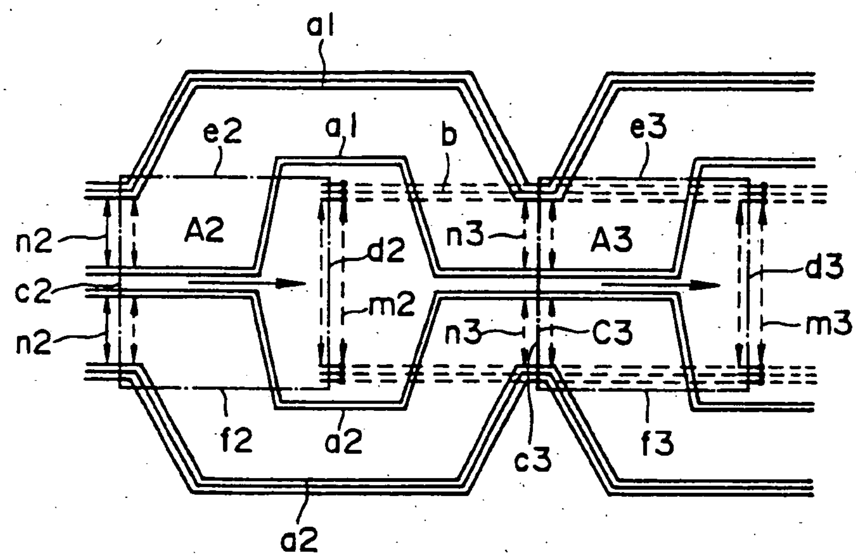


FIG.3
(PRIOR ART)

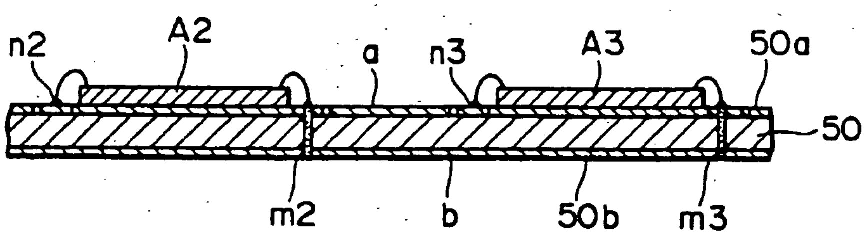


FIG.4

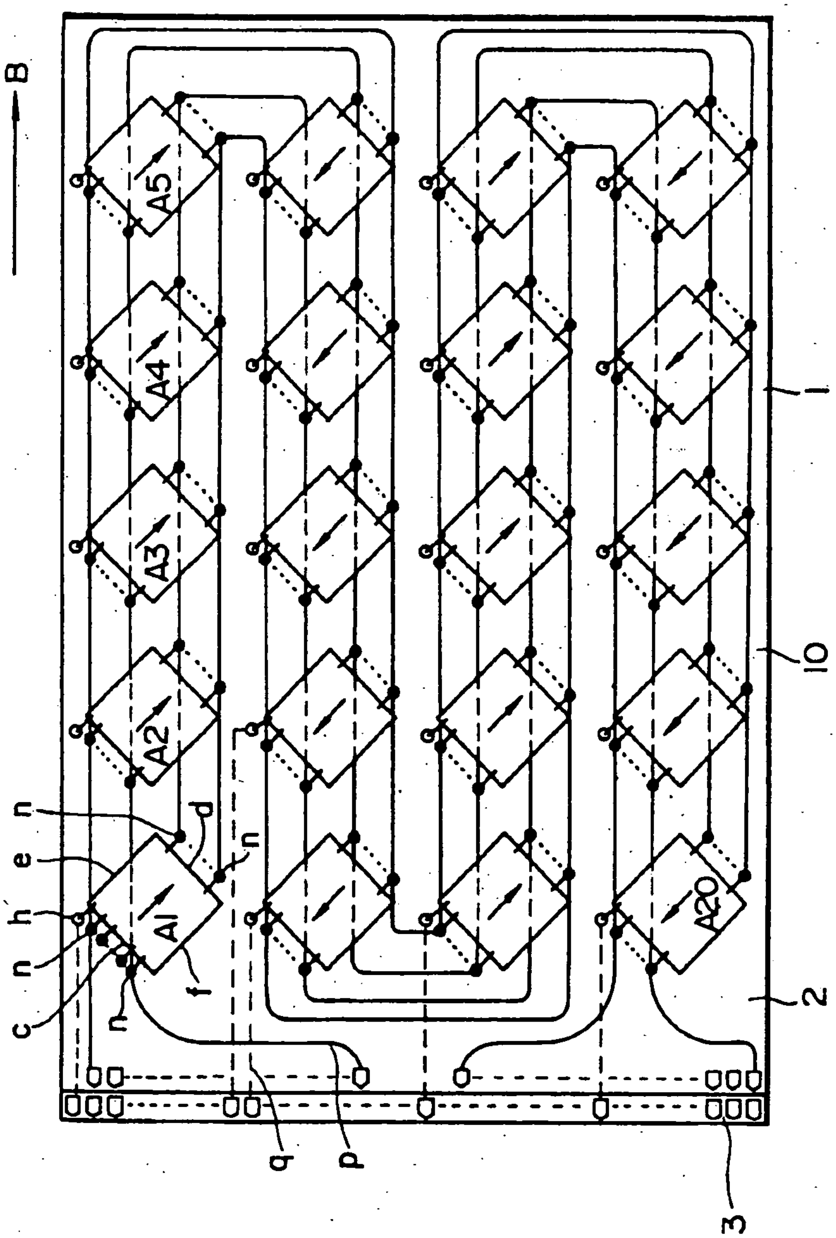


FIG.5

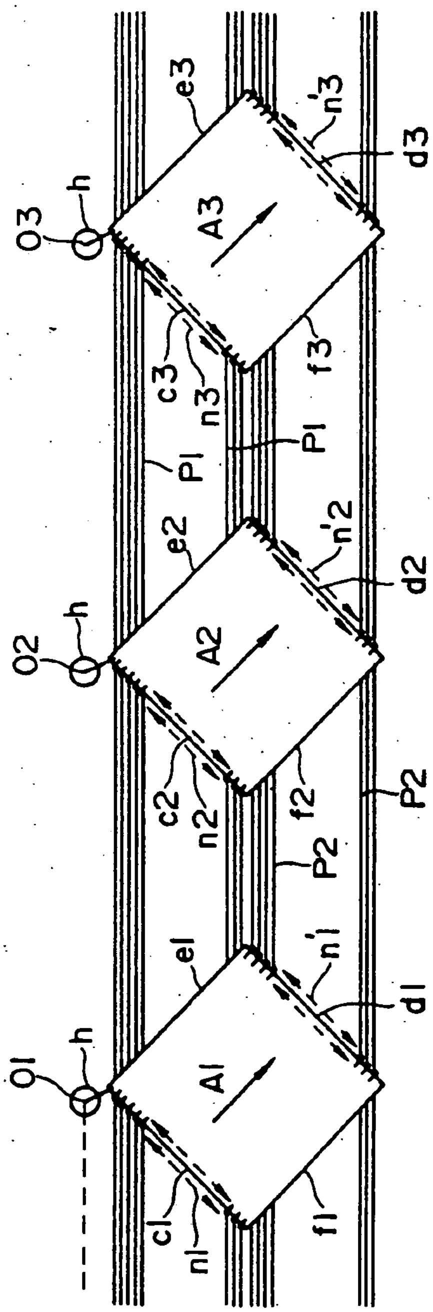

O1
h
A1
c1
n1
e1
n'1
d1
f1
P2
O2
A2
c2
n2
e2
n'2
d2
f2
P1
O3
A3
c3
n3
e3
n'3
d3
f3

FIG.6

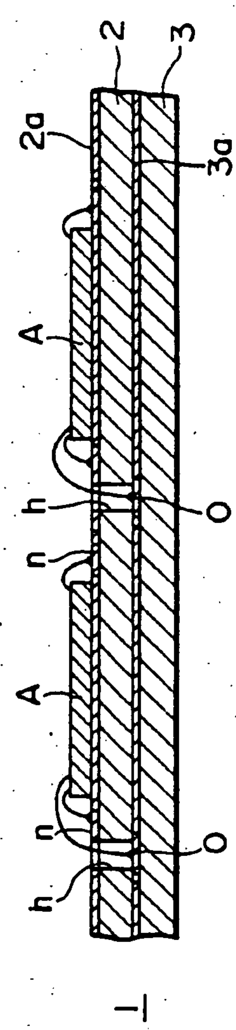
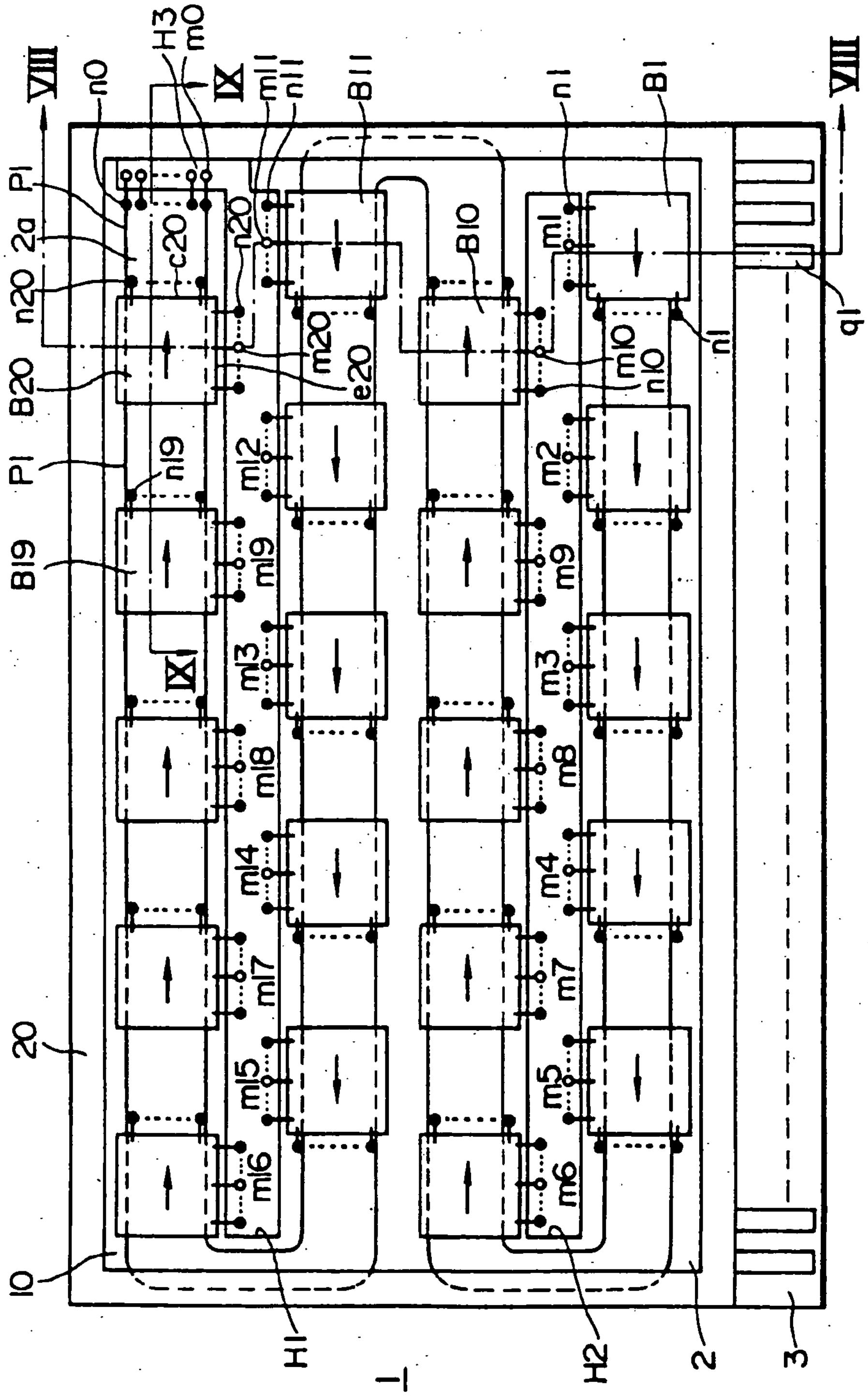

2
3
2a
3a
A
h
n
O
1

FIG. 7


VIII
VIII
IX
IX
H3
m0
n0
P1
2a
n20
B20
n19
B19
c20
n20
m20
e20
m11
n11
B11
B10
m10
n10
n1
B1
m1
n1
q1
m2
m3
m4
m5
m6
m7
m8
m9
m12
m13
m14
m15
m16
m17
m18
m19
20
10
H1
H2
1
2
3

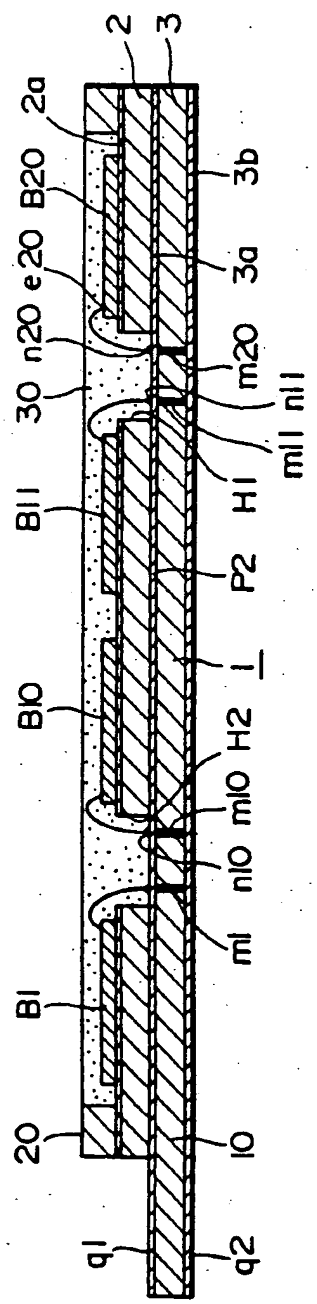

2a
B20
e20
n20
30
B11
B10
B1
20
q1
2
3
3b
3a
m20
m11 n11
m11
H1
P2
1
H2
m10
n10
m1
10
q2

FIG.8

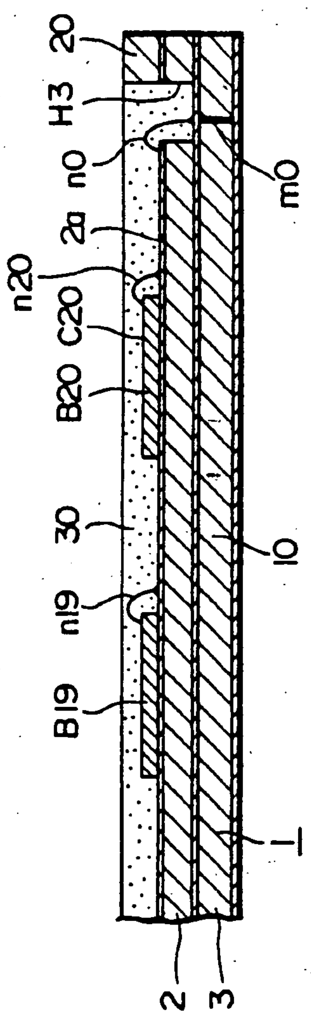

20
H3
n0
2a
n20
C20
B20
30
n19
B19
m0
10
1
2
3

FIG.9

FIG. 10

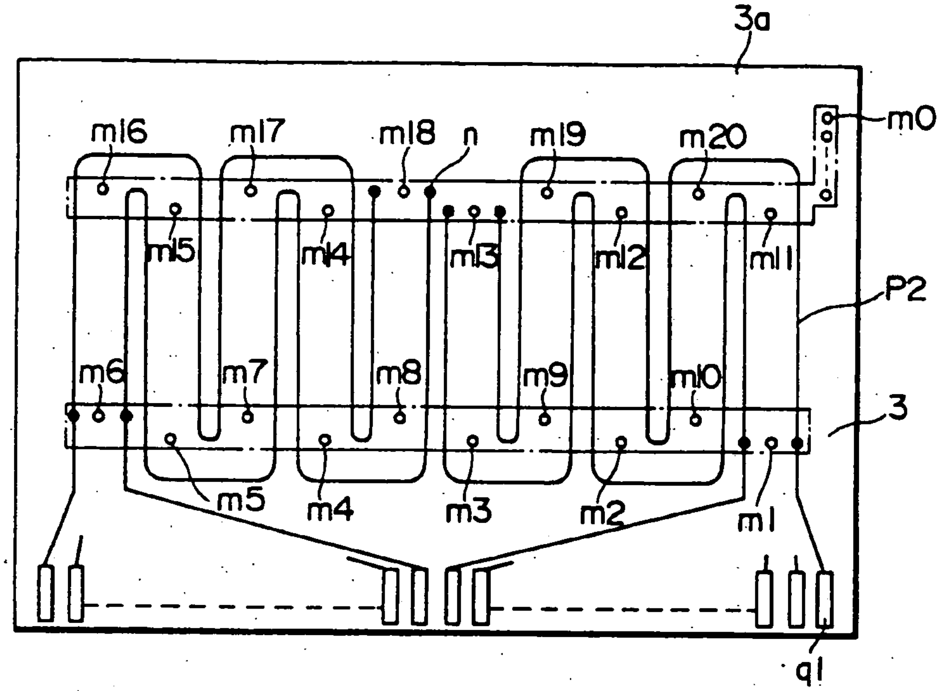

3a
m0
m16
m17
m18
n
m19
m20
m15
m14
m13
m12
m11
P2
m6
m7
m8
m9
m10
3
m5
m4
m3
m2
m1
q1

FIG. 11

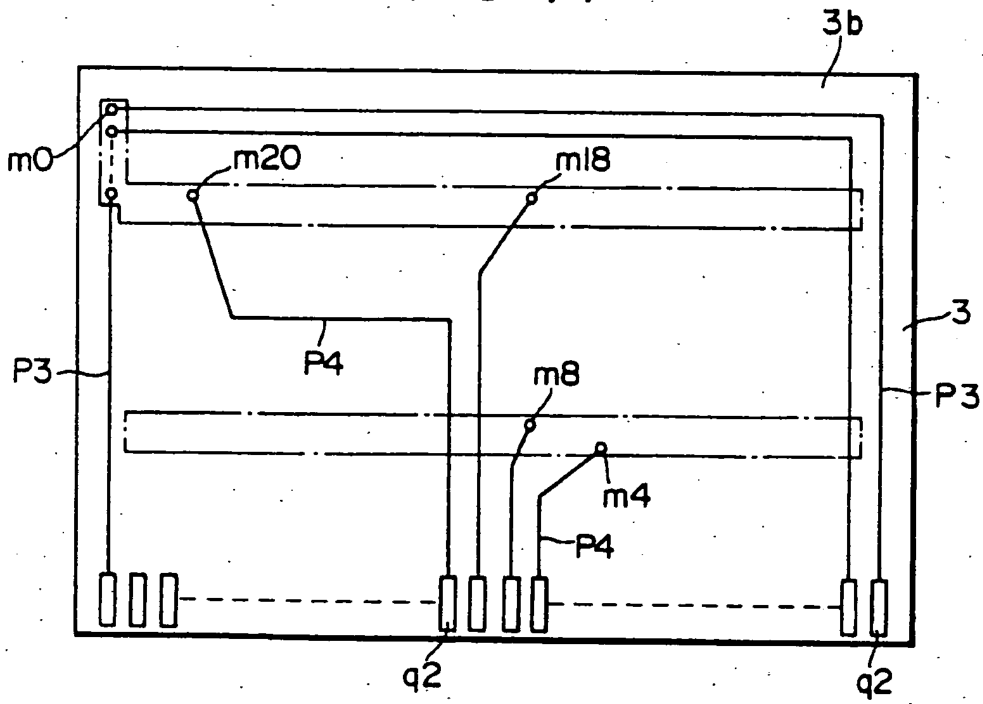

3b
m0
m20
m18
3
P4
P3
m8
P3
m4
P4
q2
q2

FIG. 12

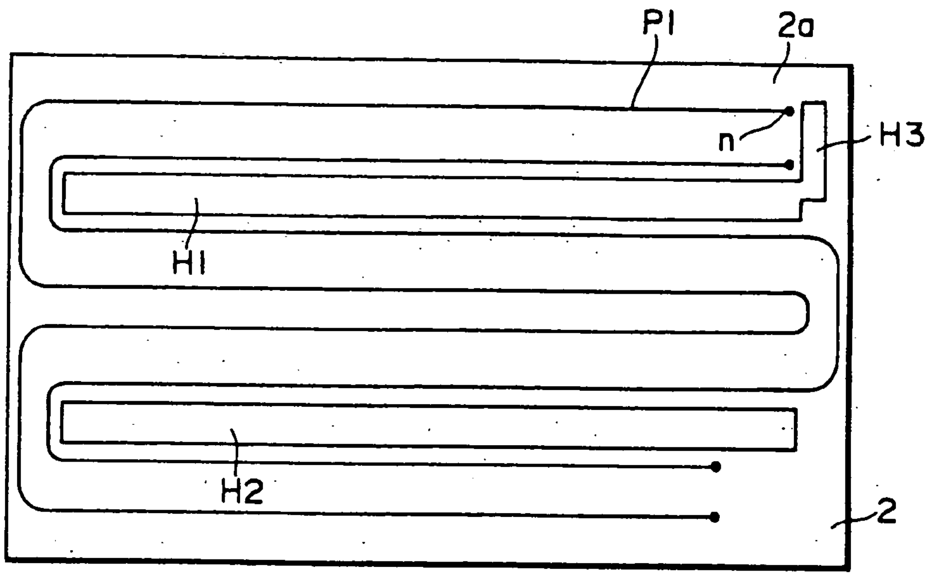


FIG. 13

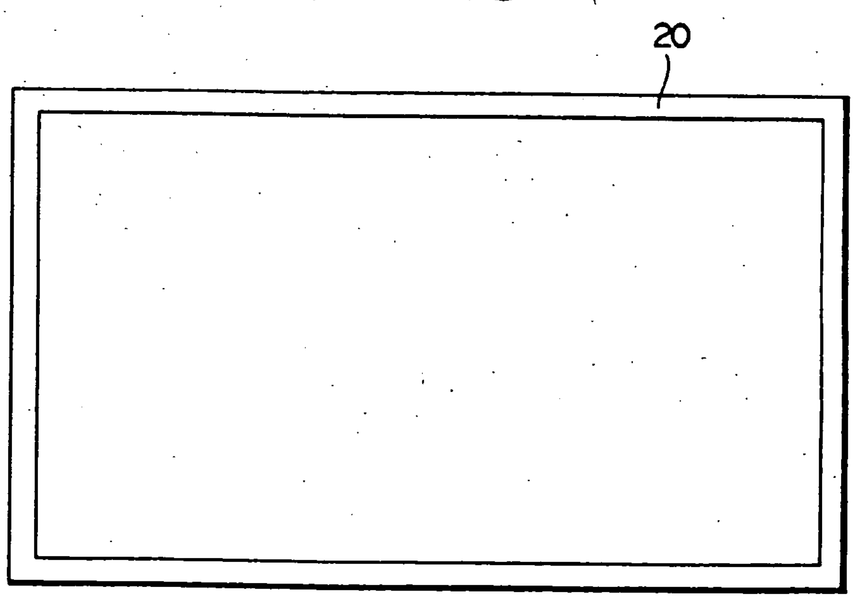


FIG. 14